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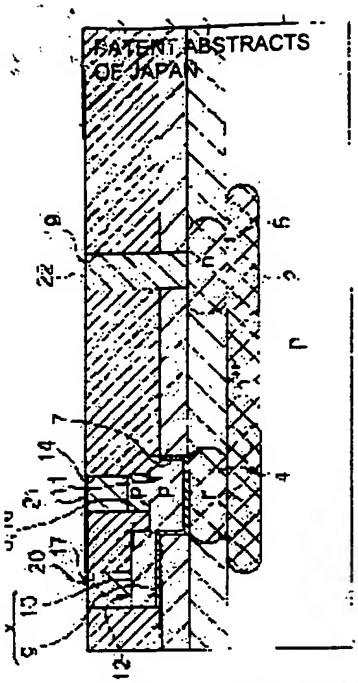

PATENT ABSTRACTS OF JAPAN

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(54) **SiGe FILM FORMING METHOD, METHOD OF MANUFACTURING HETEROJUNCTION TRANSISTOR AND HETEROJUNCTION BIPOLAR TRANSISTOR**

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent an SiGe film on an insulating film from becoming rough and to improve film quality and film resistance in an SiGe film forming method, a manufacturing method of a heterojunction transistor and a heterojunction bipolar transistor.

SOLUTION: A method for forming a SiGe film 8 on the insulating film 6 is provided with a buffer forming process for forming a first Si(1-x)Gex film 9 ($0 \leq x < 0.05$) on the insulating film and a main film forming process for forming a second Si(1-y)Gey film 10 ($0.05 \leq y < 1$) on the first Si(1-x)Gex film. The buffer forming process forms the first Si(1-x)Gex in the thickness range of 0.5 nm to 5 nm.

CLAIMS

[Claim(s)]

[Claim 1] It is the formation method of the SiGe film which is quipp d with the following and characterized by the afor mentioned buff r formation process forming Si(1-x) Gex film of the above 1st in [0.5nm or more / thickness] 5nm or less. The buffer formation process which is the method of forming a SiGe film on an insulator layer, and forms 1st Si(1-x) Gex film (0<=x<0.05) on the aforementioned insulator layer. The main film formation process which forms 2nd Si(1-y) Gey film (0.05<=y<1) on Si(1-x) Gex film of the above 1st.

[Claim 2] The formation method of the SiGe film which is the formation method of a SiGe film according to claim 1, and is characterized by forming Si(1-y) Gey film of the above 2nd by the reduced pressur CVD of 0.133Pa or more pressure range 1.33x104Pa or less at least.

[Claim 3] It is the manufacture method of the heterojunction transistor which is equipped with the following and characterized by the aforementioned SiGe film formation process forming the aforementioned SiGe film by the formation method of a SiGe film according to claim 1 or 2. The process which forms an insulator layer on Si substrate in which it is the method of manufacturing the heterojunction transistor which has the base region of SiGe, and the collector field was formed. The process which forms in a part of aforementioned insulator layer the window part which leads to the aforementioned collector field. The SiGe film formation process which forms the field with which the outgoing line to a base electrode is presented on the aforementioned insulator layer while forming a SiGe film in un-choosing on the aforementioned window part and the aforementioned insulator layer and forming the aforementioned base region on a window part. The process which forms the emitter r gion of Si on the aforementioned base region.

[Claim 4] The aforementioned SiGe film formation process is the manufacture method of a het rojunction transistor that it is characterized by germanium composition ratio y of Si(1-y) Gey film of the above 2nd being within the limits of 0.08<=y<=0.3 in the method of manufacturing a heterojunction transistor according to claim 3.

[Claim 5] 1st Si(1-x) Gex film with which it had the following and the aforementioned outgoing line at least was formed on the aforementioned insulator layer (0<=x<0.05), It is the heterojunction transistor which is equipped with 2nd Si(1-y) Gey film (0.05<=y<1) formed on Si(1-x) Gex film of the above 1st, and is characterized by Si(1-x) Gex film of the above 1st being 0.5nm or more thickness of 5nm or less. The collector field which is the heterojunction transistor which has the base region of SiGe, and was formed in Si substrate. An insulator layer with the window part which is formed on the aforementioned Si substrate and leads to the aforementioned collector field. The base region which is formed on the aforementioned window part and consists of a SiGe film. The emitter region of the outgoing line which consists of a SiGe film which was formed on the aforementioned insulator layer and connected to the aforementioned base region, and Si formed on the aforementioned base region.

[Claim 6] Si(1-y) Gey film of the above 2nd is a heterojunction transistor to which it is characterized by germanium composition ratio y being within the limits of 0.08<=y<=0.3 in a heterojunction transistor according to claim 5.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The t chnical field to which inv ntion belongs] this invention relates to the formation method of a SiG film and the manufactur method of a heterojunction transistor suitable as a base outgoing lin for xample, in a heterojunction transistor, and a het rojunction bipolar transistor.

[0002]

[Description of the Prior Art] By nlarging the band gap of an emitt r r gion and raising emitt r inj ction effici ncy sharply rather than a bas region, in low noise and Si, th high-spe d operation which cannot be attain d is possible for HBT (het rojunction transistor) which aims at incr ase of a current gain, and

it is a highly efficient device used for a logical circuit, communication syst m, microwave devices (amplifier used for A/D conversion), etc.
[0003] Conv ntionally, although HBT was manufactured by th combination of GaAs and AlGaAs etc., since the band gap of SiGe (silicon-germanium) is smaller than Si (silicon), th development research of the HBT (SiGe-HBT is called hereafter) using SiGe is carried out in recent years. This SiGe-HBT has the advantage of it not being necessary to use As with treatment difficult in environment etc. so much compared with Si in which a manufacturing cost falls compared with the possibility of mixed loading (formation of 1 chip) with abundant Si processes of technical accumulation, and Si-LSI which is easy to adjust, and a GaAs device etc.
[0004] After forming SiO2 on the silicon wafer with which the collector field was formed as a manufacture process of SiGe-HBT which uses SiGe for a base region, for example, preparing base opening (base window part) to this SiO2, growing SiGe epitaxially to this base opening and forming a base region, the emitter region of Si is formed on a base region.
[0005] In addition, in the former, for example, JP,9-181091,A, and JP,2000-31155,A, before performing non-choosing epitaxial growth of SiGe, the technology which forms 10-50nm of Si as a buffer is indicated. moreover, for example D. L.Harame, etc. J(IEEE Transactions on Electron Devices, Vol.42, No., March 1995, p469.).L.Regolini (), etc. [Materials] In Science in Semiconductor Processing The technology of performing non-choosing epitaxial growth of SiGe is proposed without exfoliating a polycrystal Si thin film, after depositing a polycrystal Si thin film all over a wafer and **********ing the insulator layer of the base section by making this into a mask, in case base opening is processed.
[0006]
[Problem(s) to be Solved by the Invention] However, the following technical problems are left behind in the above-mentioned Prior art. In SiGe-HBT which makes SiGe form by non-choosing epitaxial growth, while the epitaxial layer which grows up to be base opening is used as a base layer (base region), the polycrystal layer which grows on SiO2 succeeding a base layer is used as a base outgoing line. In this case, if direct SiGe is formed on SiO2, the polycrystal layer which grows on SiO2 will start a film dry area, resistance of a base outgoing line becomes high as a result, and transistor characteristics may be degraded. A film dry area tends to produce higher germanium composition ratio especially required of the base region of HBT, and there is an inclination for the effect to tend to become remarkable, so that thickness is thin.
[0007] Since 10-50nm of buffer layers of Si is beforehand formed on SiO2, although it is thought with the above-mentioned conventional technology that it is hard to produce the film dry area of SiGe which grows on it, when using this buffer layer as a base layer, base thickness will become thick substantially by 10-50nm of buffer thickness. That is, with the conventional technology, the electronic base transit time's having become long, and the merit which adopted the SiGe base layer for high-speed operation having reduced only the part of buffer thickness, and having un-arranged [which becomes slower than the case where the working speed of a transistor forms a base region only by SiGe], although base **** of a transistor generally became such a high-speed transistor that it is thin.
[0008] moreover, a polycrystal Si thin film -- a mask -- carrying out -- the insulator layer of the base section -- etching -- although a manufacturing process which is different by membrane formation of Polycrystal Si and membrane formation of SiGe is needed with the above-mentioned conventional technology perform SiGe growth behind the bottom, many [like / it is necessary to suppress the heat history in a manufacturing process as much as possible, and / this conventional technology from a viewpoint of the thermal effect to a device / as a heat process] makes it fond, it is, and are not things in LSI manufacture in recent years as a result of
[0009] this invention aims at offering the formation method of a SiGe film that it was able to be made in view of the above-mentioned technical problem, it can prevent the SiGe film on an insulator layer being ruined, and membraneous quality and a membrane resistance can be improved, the manufacture method of a heterojunction transistor, and a heterojunction bipolar transistor.
[0010]
[Means for Solving the Problem] As a result of having inquired about the membrane formation technology of SiGe, when this inv ntion persons w re germanium composition ratios of th fixed rang , they found out that v ry thin SiGe buffer thickness could also improve a film dry area and r sistanc sharply. That is, this invention p rsons grew the SiGe film into which buffer layer thickness was changed, and measured the r sistance whil they grew the SiG film which changed germanium

composition ratio on SiO2 and inv stigat d the membran formation stat tc. In addition, drawing 5 , drawing 6 , and drawing 7 ar the SEM photographs of the SiGe film which carri d out germanium composition ratio to 0.04, and 0.13 and 0.30, r sp ctively. Mor over, drawing 8 is an example of a resistance m asur ment and is a graph which shows sh t resistance of the SiG film (the thickness on g rmanium composition ratio 0.30 and a buffer layer is the sam) at the tim of growing up Si film as a buffer layer on SiO2, and changing the thickness of this buffer layer to 0-5nm.

[0011] As drawing 6 - drawing 7 show, in the case where germanium composition ratio is 0.13, it turns out that a SiGe film is discontinuity-ized partially, it discontinuity-izes completely in the case of g rmanium composition ratio 0.30, and it does not discontinuity-ize on the whole by the case of 0.04 to membranes hardly being formed, but the good membrane formation state is acquired further. Moreover, as drawing 8 shows, it turns out that resistance is reduced for the thickness of a buffer layer by the abbreviation half by 0.5nm, and resistance falls [thickness] by 1 figure in 1nm further.

[0012] Therefore, this invention was the technology based on this knowledge, and the following composition was used for it in order to solve the aforementioned technical problem. Namely, the formation method of the SiGe film of this invention The buffer formation process which is the method of forming a SiGe film on an insulator layer, and forms 1st Si(1-x) Gex film (0<=x<0.05) on the aforementioned insulator layer, It has the main film formation process which forms 2nd Si(1-y) Gey film (0.05<=y<1) on Si(1-x) Gex film of the above 1st, and the aforementioned buffer formation process is characterized by forming Si(1-x) Gex film of the above 1st in [0.5nm or more / thickness] 5nm or less.

[0013] Since 1st Si(1-x) Gex film is formed in [0.5nm or more / thickness] 5nm or less, the thick buffer layer of 10-50nm can be made unnecessary like before, discontinuous-ization (film dry area) of the 2nd SiGe film can be improved by the very thin buffer layer, and resistance can also be made to resist sharply in a buffer formation process by the formation method of this SiGe film. In addition, if 1st Si(1-x) Gex film is set to at least 0.5nm as mentioned above, the effect of reducing resistance sharply rather than the case (only 2nd Si(1-y) Gey film) where 1st Si(1-x) Gex film is not prepared at all will be acquired. For example, if 1st Si(1-x) Gex film is set to 0.5nm even if 2nd Si(1-y) Gey film is germanium composition ratio y= 0.3, resistance can be reduced in an abbreviation half, and more preferably if 1nm, 1 figure of resistance can be lowered. In addition, having set 1st Si(1-x) Gex film to 5nm or less has the small effect of the reduction in resistance, even if it thickens more than this, and it is for resistance to seldom change.

[0014] Moreover, at least, the formation method of the SiGe film of this invention is suitable, when forming Si(1-y) Gey film of the above 2nd by the reduced pressure CVD of 0.133Pa or more pressure range 1.33x104Pa or less. That is, although reduced pressure CVD has a possibility that the film dry area of a SiGe film may become remarkable rather than the UHV-CVD which forms membranes by the high vacuum, it can acquire the effect of film dry-area suppression notably compared with the growth methods, such as UHV-CVD, by applying reduced pressure CVD to the membrane formation method of 2nd Si(1-y) Gey film of this invention. Moreover, since reduced pressure CVD can also obtain a good SiGe film easily, they are quantities, such as UHV-CVD.

[0015] The manufacture method of the heterojunction transistor of this invention The process which forms an insulator layer on Si substrate in which it is the method of manufacturing the heterojunction transistor which has the base region of SiGe, and the collector field was formed, The process which forms in a part of aforementioned insulator layer the window part which leads to the aforementioned collector field, The SiGe film formation process which forms the field with which the outgoing line to a base electrode is presented on the aforementioned insulator layer while forming a SiGe film in un-choosing on the aforementioned window part and the aforementioned insulator layer and forming the aforementioned base region on a window part, It has the process which forms the emitter region of Si on the aforementioned base region, and the aforementioned SiGe film formation process is characterized by forming the aforementioned SiGe film by the formation method of the SiGe film of the above-mentioned this inv ntion.

[0016] Mor over, the coll ctor field which the heterojunction transistor of this inv ntion is a heterojunction transistor which has the bas r gion of SiG , and was formed in Si substrate, An insulator layer with the window part which is formed on the afor m ntion d Si substrate and leads to the aforemention d collector fi ld, The base r gion which is form d on the afor m ntion d window part and consists of a SiGe film, and the outgoing line which consists of a SiGe film which was formed on the aforemention d insulator lay r and connect d to the aforem ntion d base region, It has the emitter

r gion of Si form d on th afor m ntion d bas r gion. at l ast the aforementioned outgoing line 1st Si(1-x) Gex film formed on the afor m ntion d insulator layer (0<=x<0.05), It has 2nd Si(1-y) Gey film (0.05<=y<1) form d on Si(1-x) Gex film of th above 1st, and Si(1-x) Gex film of th above 1st is characteriz d by being 0.5nm or more thickness of 5nm or less.
[0017] With th manufacture method of thes h t rojunction transistors, and a h terojunction transistor 2nd Si(1-y) Gey film (0.05<=y<1) is formed on 1st Si(1-x) Gex film (0<=x<0.05), and since 1st Si(1-x) Gex film is 0.5nm or more thickness of 5nm or less Since 1st thin Si(1-x) Gex film is used as the buff r as a SiGe film of a base region while the SiGe film with which the film dry area was suppressed is obtained and being able to carry out [low ****]-izing of the base outgoing line on an insulator layer, base **** can be made thin as a whole.
[0018] Moreover, as for the manufacture method of the heterojunction transistor of this invention, it is desirable that the aforementioned SiGe film formation process is [germanium composition ratio y of Si(1-y) Gey film of the above 2nd] within the limits of 0.08<=y<=0.3. Moreover, as for the heterojunction transistor of this invention, it is desirable that germanium composition ratio y of Si(1-y) Gey film of the above 2nd is within the limits of 0.08<=y<=0.3.
[0019] With the manufacture method of these heterojunction transistors, and a heterojunction transistor, since germanium composition ratio y of 2nd Si(1-y) Gey film is within the limits of 0.08<=y<=0.3, a band gap suitable as a base region of HBT is obtained.
[0020]
[Embodiments of the Invention] Hereafter, the formation method of the SiGe film concerning this invention, the manufacture method of a heterojunction transistor, and 1 operation gestalt of a heterojunction bipolar transistor are explained, referring to drawing 3 from drawing 1 .
[0021] Drawing 1 shows the rough cross-section structure of the heterojunction bipolar transistor silicon (HBT) of this invention. If the structure of this HBT is explained together with the manufacture process, as shown in (a) of drawing 2 , the pad sub collector field 2 doped by n++ by arsenic placing will be formed in p type silicon wafer (Si substrate) 1 front face, and the n-Si epitaxial layer 3 of n type single crystal silicon will be further formed in silicon wafer 1 front face by epitaxial growth.
[0022] Next, as shown in (b) of drawing 2 , it embeds at the n-Si epitaxial layer 3, and the 1st collector well 4 and the 2nd collector well 5 (collector field) which were doped by n+ are generated by Lynn placing so that the sub collector field 2 may be arrived at. and it is shown in (c) of drawing 2 -- as -- the front face of the n-Si epitaxial layer 3 -- as an insulator layer -- the 1st SiO two-layer (diacid-ized silicon layer) -- 6 is formed according to a thermal oxidation process then, the 1st SiO two-layer -- mask processing is performed to 6, it etches alternatively, and the base window part 7 which leads to the 1st collector well 4 is formed
[0023] Next, as shown in (d) of drawing 2 , the SiGe film 8 is formed in un-choosing on the base window part 7 and the 1st SiO two-layer 6. This SiGe film 8 has the two-layer structure of the 1st Si(1-x) Gex film (0<=x<0.05) 9 formed as a buffer layer, and the 2nd Si(1-y) Gey film (0.05<=y<1) 10 formed on this 1st Si(1-x) Gex film 9.
[0024] That is, in order to form the SiGe film 8, the 1st Si(1-x) Gex film 9 is first formed by non-choosing epitaxial growth in [0.5nm or more / thickness] 5nm or less on the base window part 7 and the 1st SiO two-layer 6 (buffer formation process). Furthermore, the 2nd Si(1-y) Gey film 10 is formed by non-choosing epitaxial growth on the 1st Si(1-x) Gex film 9.
[0025] In addition, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 form membranes by the reduced pressure CVD of 0.133Pa or more pressure range 1.33x104Pa or less. Moreover, germanium composition ratio y of the 2nd Si(1-y) Gey film 10 is more preferably set up within the limits of 0.08<=y<=0.3. Moreover, while the membrane formation temperature in this reduced pressure CVD is 600-800 degrees C, H2 is used as carrier gas and SiH4 and GeH4 are used as source gas.
[0026] At this membrane formation process, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 with which the 1st Si(1-x) G x film 9 and the 2nd Si(1-y) Gey film 10 which ar formed in the base window part 7 are formed as an pitaxial layer of a single crystal, and are formed on the 1st SiO two-layer 6 are formed as a non- pitaxial layer of a polycrystal. In addition, the 1st Si(1-x) G x film 9 and the 2nd Si(1-y) Gey film 10 are doped by p by boron. Thus, the base region 11 of the h terojunction by the SiGe film 8 is form d in th bas window part 7.
[0027] Next, as mask processing is p rform d on the 2nd Si(1-y) G y film 10, it etches alternativ ly and it is shown in (a) of drawing 3 , it leaves the portion with which the base outgoing line 12 and a base

region 11 are presented, and the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 are removed. furthermore, the xposed 2nd Si(1-y) Gey film [which remain d as shown in (b) of drawing 3] 10, and 1st SiO two-layer the 6 top -- the 2nd SiO two-layer -- 13 is form d

[0028] Next, on the 2nd SiO two-layer 13, mask processing is perform d, w t tching is performed alt rnatively, and the mitter window part 14 which leads to a base r gion 11 is formed. Th n, on the emitter window part 14 and the 2nd SiO two-layer 13, Si is grown epitaxially by CVD, Si single crystal lay r 15 is formed to the emitter window part 14, and an emitter region 16 is formed. And mask processing is performed to the emitter window part 14, it leaves the portion with which an emitter region 16 is presented, and etching processing removes Si on the 2nd SiO two-layer 13.

[0029] Next, mask processing is performed on the 2nd SiO two-layer 13, wet etching is performed alternatively, and as shown in (c) of drawing 3 , the base-electrode window part 17 which leads to th base outgoing line 12, the emitter electrode window part 18 which leads to an emitter region 16, and the collector-electrode window part 19 which leads to the 2nd collector well 5 are formed. Then, HBT of this operation gestalt is manufactured by embedding a metallic material alternatively at the base-electrode window part 17, the emitter electrode window part 18, and the collector-electrode window part 19, and forming a base electrode 20, the emitter electrode 21, and a collector electrode 22, respectively.

[0030] In the formation method of the SiGe film of this operation gestalt, the manufacture method of HBT, and HBT The 2nd Si(1-y) Gey film 10 (0.05<=y<1) is formed on the 1st Si(1-x) Gex film 9 (0<=x<0.05), and since the 1st Si(1-x) Gex film 9 is 0.5nm or more thickness of 5nm or less While th SiGe film 8 with which the film dry area was suppressed is obtained and being able to carry out [low ****]-izing of the base outgoing line 12 on the 1st SiO two-layer 6, as a SiGe film 8 of a base region 11 Since the 1st thin Si(1-x) Gex film 9 is used as the buffer, as a whole, base **** becomes thin and can obtain high-speed operation.

[0031] moreover, since it is the reduced pressure CVD of 0.133Pa or more pressure range 1.33x104Pa or less, the 2nd Si(1-y) Gey film 10 is formed and reduced pressure CVD can also obtain a good SiGe film easily while being able to acquire the effect of film dry-area suppression notably compared with the growth methods, such as UHV-CVD, the need of using high-vacuum technology, such as UHV-CVD, can be lost, and productivity etc. can be raised In addition, since germanium composition ratio y of the 2nd Si(1-y) Gey film 10 is within the limits of 0.08<=y<=0.3, a band gap suitable as a base region 11 of HBT is obtained.

[0032]

[Example] Next, an example explains concretely the formation method of the SiGe film concerning this invention, the manufacture method of a heterojunction transistor, and a heterojunction bipolar transistor.

[0033] 1st Si(1-x) Gex film and 2nd Si(1-y) Gey film were actually formed on SiO two-layer [1st] lik the above-mentioned operation gestalt, and the membrane formation state and resistance (sheet resistance) were investigated. In addition, germanium composition ratio y of 2nd Si(1-y) Gey film of the example concerning this invention is 0.30. Moreover, thickness is 5nm and, as for 1st Si(1-x) Gex film, g rmanium composition ratio uses 0, i.e., Si film.

[0034] Drawing 4 shows the SEM photograph of the SiGe film by the example of this invention. Wh n this drawing 4 is compared with drawing 7 as an example of comparison, by the case of this exampl , it turns out that continuation and the good membrane formation state are acquired to SiGe discontinuity-izing in the case of the example of comparison which does not have a buffer layer, and membranes hardly being formed.

[0035] Moreover, when the sheet resistance at the time of forming a SiGe layer (germanium composition ratio 0.30) was investigated, as shown in drawing 8 , to having been 1x105ohms, in th example of this invention, in the case of a SiGe layer without a buffer layer, it is 1x104ohms, and it had also formed 1 figur into low resistance. Thus, in the case wh re this inv ntion is applied, whil the good film was obtained compar d with the former, large low resistance-ization was obtain d.

[0036] In addition, this invention also includes the following operation g stalt n. With th above-m ntion d op ration gestalt, although the formation method of th SiGe film of this inv ntion was applied to th bas outgoing-lin formation in HBT, you may apply to manufactur of oth r d vices which have th structure which formed th SiGe film on the insulator layer. For exampl , in MOS structur s, such as an MOS transistor, when forming a SiG film as a gate electrode on a gate oxide

film, you may apply this inv ntion.
[0037] Moreov r, although g rmanium composition ratio formed the fix d layer as 1st SiGe film with the above-mention d op ration g stalt, the 1st SiGe film which is changing within the limits of 0<=x<0.05 is suffici nt as g rmanium composition ratio x. For example, it is contained in this invention, when the SiGe layer toward which composition inclined is form d and germanium composition ratio x forms the SiGe layer of 0.15 further on the SiGe layer of this inclination composition, making germanium composition ratio x increase gradually from 0 to 0.15 on an insulator layer (SiO2).
[0038] That is, if the field of the layer which has early germanium composition ratio x of 0<=x<0.05 among the inclination composition SiGe layers formed on an insulator layer is 0.5nm <= 5nm or less in thickness, the field of this layer can regard it as the 1st SiGe film in this invention. And germanium composition ratio x after this field can consider that the SiGe fields from 0.05 to 0.15 are the 2nd SiGe film in this invention. Thus, the 2nd SiGe film which forms membranes on the 1st SiGe film in this invention also contains the SiGe layer formed continuously, without interrupting a membrane formation process after membrane formation of the 1st SiGe film.
[0039]
[Effect of the Invention] According to this invention, the following effects are done so. Since 1st Si(1-x) Gex film is formed in [0.5nm or more / thickness] 5nm or less in a buffer formation process according to the formation method of the SiGe film of this invention Make unnecessary the thick buffer layer of 10-50nm like before, and discontinuous-ization (film dry area) of the 2nd SiGe film is improved by the buffer layer of very thin thickness. resistance can also be made to form into low resistance sharply, and can set the SiGe film on an insulator layer to various devices -- low -- it becomes possible to use as wiring [****] or an electrode
[0040] Moreover, according to the manufacture method of the heterojunction transistor of this invention, and the heterojunction transistor 2nd Si(1-y) Gey film (0.05<=y<1) is formed on 1st Si(1-x) Gex film (0<=x<0.05), and since 1st Si(1-x) Gex film is 0.5nm or more thickness of 5nm or less The SiGe film with which the film dry area was suppressed on the insulator layer is obtained, and the film which can be used as a low resistance base outgoing line can be obtained in spite of thin buffer thickness. Consequently, a SiGe base region can be produced now without a thick buffer layer, and non-choosing epitaxial growth can realize SiGe-HBT in which more nearly high-speed operation is possible.

[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the formation method of a SiGe film and the manufacture method of a heterojunction transistor suitable as a base outgoing line for example, in a heterojunction transistor, and a heterojunction bipolar transistor.

[Translation done.]

PRIOR ART

[Description of the Prior Art] By enlarging the band gap of an emitter region and raising emitter injection efficiency sharply rather than a base region, in low noise and Si, the high-speed operation which cannot be attained is possible for HBT (heterojunction transistor) which aims at increase of a current gain, and it is a highly efficient devic us d for a logical circuit, communication system, microwave devices (amplifier used for A/D conversion), tc.
[0003] Conventionally, although HBT was manufactur d by the combination of GaAs and AlGaAs etc., sinc the band gap of SiGe (silicon-g rmanium) is smaller than Si (silicon), the d velopm nt research of the HBT (SiGe-HBT is called h r aft r) using SiG is carried out in r cent years. This SiGe-HBT has the advantage of it not being necessary to use As with tr atment difficult in environment etc. so much

compared with Si in which a manufacturing cost falls compared with the possibility of mixed loading (formation of 1 chip) with abundant Si processes of technical accumulation, and Si-LSI which is easy to adjust, and a GaAs device etc.
[0004] After forming SiO2 on the silicon wafer with which the collector field was formed as a manufacture process of SiGe-HBT which uses SiGe for a base region, for example, preparing base opening (base window part) to this SiO2, growing SiGe epitaxially to this base opening and forming a base region, the emitter region of Si is formed on a base region.
[0005] In addition, in the former, for example, JP,9-181091,A, and JP,2000-31155,A, before performing non-choosing epitaxial growth of SiGe, the technology which forms 10-50nm of Si as a buffer is indicated. Moreover, for example, by D.L.Harame etc. and J(IEEE Transactions on Electron Devices, Vol.42, No., March 1995, p469.).L.Regolini, in case you process base opening (Materials Science in Semiconductor Processing), deposit a polycrystal Si thin film all over a wafer, and let this be a mask. The technology of performing non-choosing epitaxial growth of SiGe is proposed without exfoliating a polycrystal Si thin film, after **********ing the insulator layer of the base section.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the following effects are done so. Since 1st Si(1-x) Gex film is formed in [0.5nm or more / thickness] 5nm or less in a buffer formation process according to the formation method of the SiGe film of this invention the thick buffer layer of 10-50nm can be made unnecessary like before, discontinuous-ization (film dry area) of the 2nd SiGe film can be improved by the buffer layer of very thin thickness, resistance can also be made to form into low resistance sharply, and the SiGe film on an insulator layer can be set to various devices -- low -- it becomes possible to use as wiring [****] or an electrode
[0040] Moreover, according to the manufacture method of the heterojunction transistor of this invention, and the heterojunction transistor 2nd Si(1-y) Gey film (0.05<=y<1) is formed on 1st Si(1-x) Gex film (0<=x<0.05), and since 1st Si(1-x) Gex film is 0.5nm or more thickness of 5nm or less The SiGe film with which the film dry area was suppressed on the insulator layer is obtained, and it is thin buffer thickness. The film which can be used as a low resistance base outgoing line can be obtained. Consequently, a SiGe base region can be produced now without a thick buffer layer, and non-choosing epitaxial growth can realize SiGe-HBT in which more nearly high-speed operation is possible.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the following technical problems are left behind in the above-mentioned Prior art. In SiGe-HBT which makes SiGe form by non-choosing epitaxial growth, while the epitaxial layer which grows up to be base opening is used as a base layer (base region), the polycrystal layer which grows on SiO2 succeeding a base layer is used as a base outgoing line. In this case, if direct SiGe is formed on SiO2, the polycrystal layer which grows on SiO2 will start a film dry area, resistance of a base outgoing line becomes high as a result, and transistor characteristics may be degraded. A film dry area tends to produce higher germanium composition ratio especially required of the base region of HBT, and there is an inclination for the effect to tend to become remarkable, so that thickness is thin.
[0007] Since 10-50nm of buffer layers of Si is beforehand form d on SiO2, although it is thought with the above-mentioned conventional technology that it is hard to produce the film dry area of SiGe which grows on it, when using this buffer layer as a base layer, base thickness will becom thick substantially by 10-50nm of buffer thickn ss. That is, with the conventional technology, the electronic base transit

time's having become long, and the merit which adopted the SiGe base layer for high-speed operation = having r duc d only the part of buff r thickn ss, and having un-arrang d [which becomes slower than the case wh re th working spe d of a transistor forms a base r gion only by SiGe], although base **** of a transistor gen rally becam such a high-speed transistor that it is thin.
[0008] moreover, a polycrystal Si thin film -- a mask -- carrying out -- the insulator lay r of the base section -- etching -- although a manufacturing process which is different by membrane formation of Polycrystal Si and membrane formation of SiGe is needed with the above-mentioned conventional technology perform SiGe growth behind the bottom, many [like / it is necessary to suppress the heat history in a manufacturing process as much as possible, and / this conventional technology from a viewpoint of the thermal effect to a device / as a heat process] makes it fond, it is, and are not things in LSI manufacture in recent years as a result of
[0009] this invention aims at offering the formation method of a SiGe film that it was able to be made in view of the above-mentioned technical problem, it can prevent the SiGe film on an insulator layer being ruined, and membraneous quality and a membrane resistance can be improved, the manufacture method of a heterojunction transistor, and a heterojunction bipolar transistor.

[Translation done.]

MEANS

[Means for Solving the Problem] As a result of having inquired about the membrane formation technology of SiGe, when this invention persons were germanium composition ratios of the fixed range, they found out that very thin SiGe buffer thickness could also improve a film dry area and resistance sharply. That is, this invention persons grew the SiGe film into which buffer layer thickness was changed, and measured the resistance while they grew the SiGe film which changed germanium composition ratio on SiO2 and investigated the membrane formation state etc. In addition, drawing 5 , drawing 6 , and drawing 7 are the SEM photographs of the SiGe film which carried out germanium composition ratio to 0.04, and 0.13 and 0.30, respectively. Moreover, drawing 8 is an example of a resistance measurement and is a graph which shows sheet resistance of the SiGe film (the thickness on germanium composition ratio 0.30 and a buffer layer is the same) at the time of growing up Si film as a buffer layer on SiO2, and changing the thickness of this buffer layer to 0-5nm.
[0011] As drawing 6 - drawing 7 show, in the case where germanium composition ratio is 0.13, it turns out that a SiGe film is discontinuity-ized partially, it discontinuity-izes completely in the case of germanium composition ratio 0.30, and it does not discontinuity-ize on the whole by the case of 0.04 to membranes hardly being formed, but the good membrane formation state is acquired further. Moreover, as drawing 8 shows, it turns out that resistance is reduced for the thickness of a buffer layer by the abbreviation half by 0.5nm, and resistance falls [thickness] by 1 figure in 1nm further.
[0012] Therefore, this invention was the technology based on this knowledge, and the following composition was used for it in order to solve the aforementioned technical problem. Namely, the formation method of the SiGe film of this invention The buffer formation process which is the method of forming a SiGe film on an insulator layer, and forms 1st Si(1-x) Gex film ($0<=x<0.05$) on the aforementioned insulator layer, It has the main film formation process which forms 2nd Si(1-y) Gey film ($0.05<=y<1$) on Si(1-x) Gex film of the above 1st, and the aforementioned buffer formation process is characterized by forming Si(1-x) Gex film of the above 1st in [0.5nm or more / thickness] 5nm or less.
[0013] Since 1st Si(1-x) Gex film is formed in [0.5nm or more / thickness] 5nm or less, the thick buffer layer of 10-50nm can be made unnecessary like before, discontinuous-ization (film dry area) of the 2nd SiGe film can be improved by the very thin buffer layer, and resistance can also be made to resist sharply in a buffer formation process by the formation method of this SiGe film. In addition, if 1st Si(1-x) Gex film is set to at least 0.5nm as mentioned above, the effect of reducing resistance sharply rather than the case (only 2nd Si(1-y) Gey film) where 1st Si(1-x) Gex film is not prepared at all will be acquir d. For example, if 1st Si(1-x) Gex film is set to 0.5nm even if 2nd Si(1-y) Gey film is germanium composition ratio y= 0.3, resistance can be reduced in an abbreviation half, and more preferably if 1nm, 1 figure of resistance can be lowered. In addition, having set 1st Si(1-x) Gex film to 5nm or less has the

small eff ct of the reduction in resistance, even if it thickens more than this, and it is for resistance to seldom change.

[0014] Moreover, at least, the formation m thod of the SiGe film of this invention is suitable, when forming Si(1-y) Gey film of the above 2nd of th reduced pr ssure CVD of 0.133Pa or more pressure range 1.33x104Pa or less. That is, although r duced pressure CVD has a possibility that the film dry area of a SiGe film may become remarkable rather than the UHV-CVD which forms membranes by the high vacuum, it can acquire the effect of film dry-area suppression notably compared with the growth methods, such as UHV-CVD, by applying reduced pressure CVD to the membrane formation method of 2nd Si(1-y) Gey film of this invention. Moreover, since reduced pressure CVD can also obtain a good SiGe film easily, they are quantities, such as UHV-CVD.

[0015] The manufacture method of the heterojunction transistor of this invention The process which forms an insulator layer on Si substrate in which it is the method of manufacturing the heterojunction transistor which has the base region of SiGe, and the collector field was formed, The process which forms in a part of aforementioned insulator layer the window part which leads to the aforementioned collector field, The SiGe film formation process which forms the field with which the outgoing line to a base electrode is presented on the aforementioned insulator layer while forming a SiGe film in un-choosing on the aforementioned window part and the aforementioned insulator layer and forming th aforementioned base region on a window part, It has the process which forms the emitter region of Si on the aforementioned base region, and the aforementioned SiGe film formation process is characterized by forming the aforementioned SiGe film by the formation method of the SiGe film of the above-mentioned this invention.

[0016] Moreover, the collector field which the heterojunction transistor of this invention is a heterojunction transistor which has the base region of SiGe, and was formed in Si substrate, An insulator layer with the window part which is formed on the aforementioned Si substrate and leads to the aforementioned collector field, The base region which is formed on the aforementioned window part and consists of a SiGe film, and the outgoing line which consists of a SiGe film which was formed on the aforementioned insulator layer and connected to the aforementioned base region, It has the emitt r region of Si formed on the aforementioned base region. at least the aforementioned outgoing line 1st Si(1-x) Gex film formed on the aforementioned insulator layer ($0<=x<0.05$), It has 2nd Si(1-y) Gey film ($0.05<=y<1$) formed on Si(1-x) Gex film of the above 1st, and Si(1-x) Gex film of the above 1st is characterized by being 0.5nm or more thickness of 5nm or less.

[0017] With the manufacture method of these heterojunction transistors, and a heterojunction transistor 2nd Si(1-y) Gey film ($0.05<=y<1$) is formed on 1st Si(1-x) Gex film ($0<=x<0.05$), and since 1st Si(1-x) Gex film is 0.5nm or more thickness of 5nm or less Since 1st thin Si(1-x) Gex film is used as the buff r as a SiGe film of a base region while the SiGe film with which the film dry area was suppressed is obtained and being able to carry out [low ****]-izing of the base outgoing line on an insulator layer, base **** can be made thin as a whole.

[0018] Moreover, as for the manufacture method of the heterojunction transistor of this invention, it is desirable that the aforementioned SiGe film formation process is [germanium composition ratio y of Si(1-y) Gey film of the above 2nd] within the limits of $0.08<=y<=0.3$. Moreover, as for the heterojunction transistor of this invention, it is desirable that germanium composition ratio y of Si(1-y) Gey film of the above 2nd is within the limits of $0.08<=y<=0.3$.

[0019] With the manufacture method of these heterojunction transistors, and a heterojunction transistor, since germanium composition ratio y of 2nd Si(1-y) Gey film is within the limits of $0.08<=y<=0.3$, a band gap suitable as a base region of HBT is obtained.

[0020]

[Embodiments of the Invention] Hereafter, the formation method of the SiGe film concerning this inv ntion, the manufacture method of a heterojunction transistor, and 1 operation gestalt of a heterojunction bipolar transistor are explained, referring to drawing 3 from drawing 1 .

[0021] Drawing 1 shows the rough cross-section structure of the heterojunction bipolar transistor silicon (HBT) of this invention. If the structure of this HBT is xplained togeth r with the manufactur process, as shown in (a) of drawing 2 , the pad sub coll ctor field 2 doped by n++ by arsenic placing will b formed in p type silicon wafer (Si substrat) 1 front face, and th n-Si pitaxial layer 3 of n type single crystal silicon will be further formed in silicon wafer 1 front face by pitaxial growth.

[0022] Next, as shown in (b) of drawing 2 , it embeds at th n-Si pitaxial layer 3, and th 1st coll ctor

well 4 and the 2nd coll ctor well 5 (collector field) which w re doped by n+ are gen rated by Lynn placing so that the sub collector field 2 may be arrived at. and it is shown in (c) of drawing 2 -- as -- the front face of the n-Si epitaxial layer 3 -- as an insulator layer -- the 1st SiO two-layer (diacid-ized silicon layer) -- 6 is formed according to a thermal oxidation proc ss th n, the 1st SiO two-layer -- mask processing is p rformed to 6, it tches alternatively, and the base window part 7 which leads to the 1st collector well 4 is formed

[0023] Next, as shown in (d) of drawing 2 , the SiGe film 8 is formed in un-choosing on the base window part 7 and the 1st SiO two-layer 6. This SiGe film 8 has the two-layer structure of the 1st Si(1-x) Gex film (0<=x<0.05) 9 formed as a buffer layer, and the 2nd Si(1-y) Gey film (0.05<=y<1) 10 formed on this 1st Si(1-x) Gex film 9.

[0024] That is, in order to form the SiGe film 8, the 1st Si(1-x) Gex film 9 is first formed by non-choosing epitaxial growth in [0.5nm or more / thickness] 5nm or less on the base window part 7 and the 1st SiO two-layer 6 (buffer formation process). Furthermore, the 2nd Si(1-y) Gey film 10 is formed by non-choosing epitaxial growth on the 1st Si(1-x) Gex film 9.

[0025] In addition, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 form membranes by the reduced pressure CVD of 0.133Pa or more pressure range 1.33x104Pa or less. Moreover, germanium composition ratio y of the 2nd Si(1-y) Gey film 10 is more preferably set up within the limits of 0.08<=y<=0.3. Moreover, while the membrane formation temperature in this reduced pressure CVD is 600-800 degrees C, H2 is used as carrier gas and SiH4 and GeH4 are used as source gas.

[0026] At this membrane formation process, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 with which the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 which are formed in the base window part 7 are formed as an epitaxial layer of a single crystal, and are formed on the 1st SiO two-layer 6 are formed as a non-epitaxial layer of a polycrystal. In addition, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 are doped by p by boron. Thus, the base region 11 of the heterojunction by the SiGe film 8 is formed in the base window part 7.

[0027] Next, as mask processing is performed on the 2nd Si(1-y) Gey film 10, it etches alternatively and it is shown in (a) of drawing 3 , it leaves the portion with which the base outgoing line 12 and a base region 11 are presented, and the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 are removed. furthermore, the exposed 2nd Si(1-y) Gey film [which remained as shown in (b) of drawing 3] 10, and 1st SiO two-layer the 6 top -- the 2nd SiO two-layer -- 13 is formed

[0028] Next, on the 2nd SiO two-layer 13, mask processing is performed, wet etching is performed alternatively, and the emitter window part 14 which leads to a base region 11 is formed. Then, on the mitter window part 14 and the 2nd SiO two-layer 13, Si is grown epitaxially by CVD, Si single crystal layer 15 is formed to the emitter window part 14, and an emitter region 16 is formed. And mask processing is performed to the emitter window part 14, it leaves the portion with which an emitter region 16 is presented, and etching processing removes Si on the 2nd SiO two-layer 13.

[0029] Next, mask processing is performed on the 2nd SiO two-layer 13, wet etching is performed alternatively, and as shown in (c) of drawing 3 , the base-electrode window part 17 which leads to the base outgoing line 12, the emitter electrode window part 18 which leads to an emitter region 16, and the collector-electrode window part 19 which leads to the 2nd collector well 5 are formed. Then, HBT of this operation gestalt is manufactured by embedding a metallic material alternatively at the base-electrode window part 17, the emitter electrode window part 18, and the collector-electrode window part 19, and forming a base electrode 20, the emitter electrode 21, and a collector electrode 22, respectively.

[0030] In the formation method of the SiGe film of this operation gestalt, the manufacture method of HBT, and HBT The 2nd Si(1-y) Gey film 10 (0.05<=y<1) is formed on the 1st Si(1-x) Gex film 9 (0<=x<0.05), and since the 1st Si(1-x) Gex film 9 is 0.5nm or more thickness of 5nm or less While the SiGe film 8 with which the film dry area was suppressed is obtained and being able to carry out [low ****]-izing of the bas outgoing line 12 on the 1st SiO two-lay r 6, as a SiGe film 8 of a base region 11 Since the 1st thin Si(1-x) Gex film 9 is used as the buffer, as a whole, base **** becom s thin and can obtain high-spe d op ration.

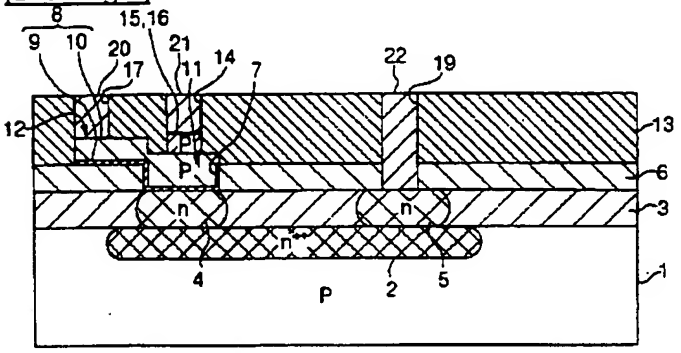
[0031] moreover, since it is the reduced pressure CVD of 0.133Pa or more pressure range 1.33x104Pa or less, the 2nd Si(1-y) G y film 10 is formed and reduced pressur CVD can also obtain a good SiG film easily while being able to acquire the effect of film dry-area suppression notably compared with the growth methods, such as UHV-CVD, th need of using high-vacuum technology, such as UHV-CVD,

can be lost, and productivity etc. can be raised In addition, since germanium composition ratio y of the 2nd Si(1-y) Gey film 10 is within the limits of 0.08<=y<=0.3, a band gap suitable as a base region 11 of HBT is obtained.

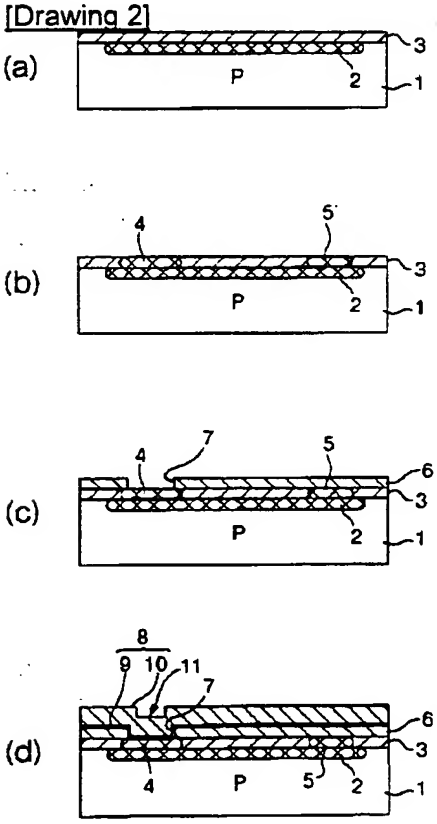
[Translation done.]

DRAWINGS

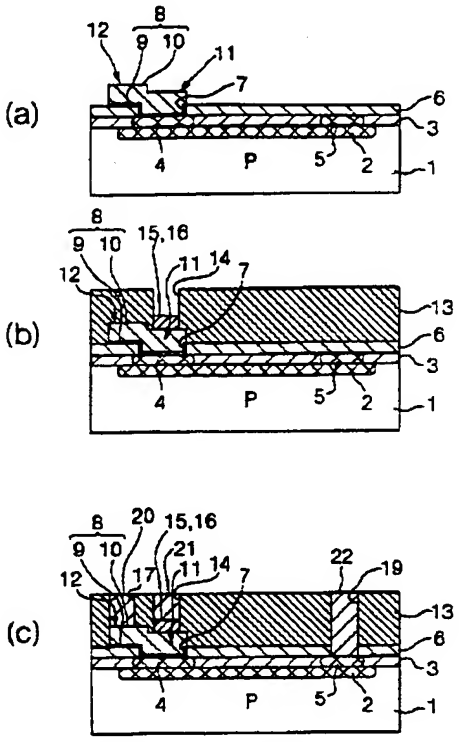
[Drawing 1]



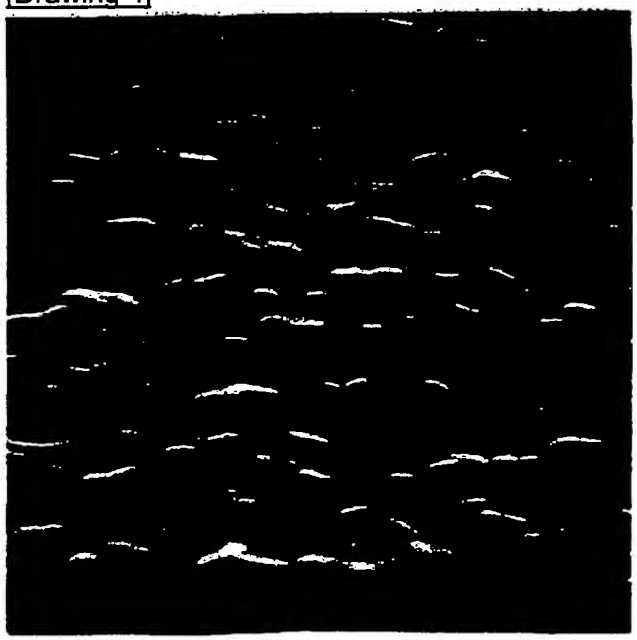
[Drawing 2]



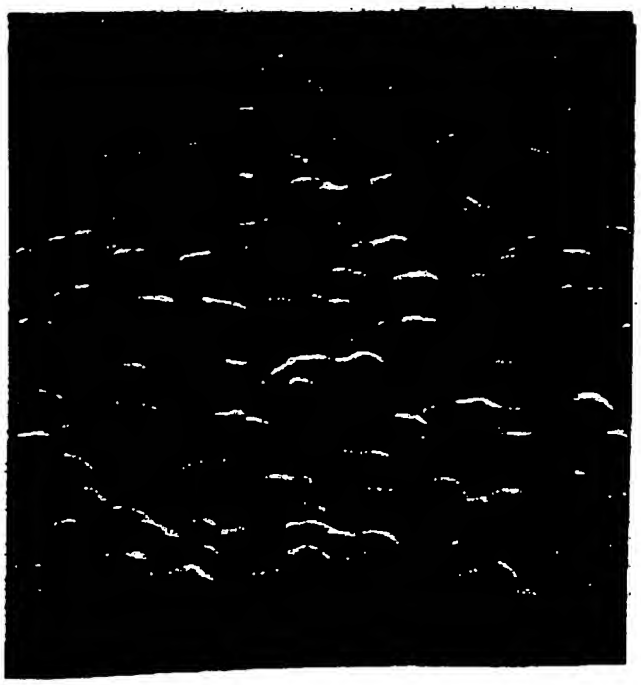
[Drawing 3]



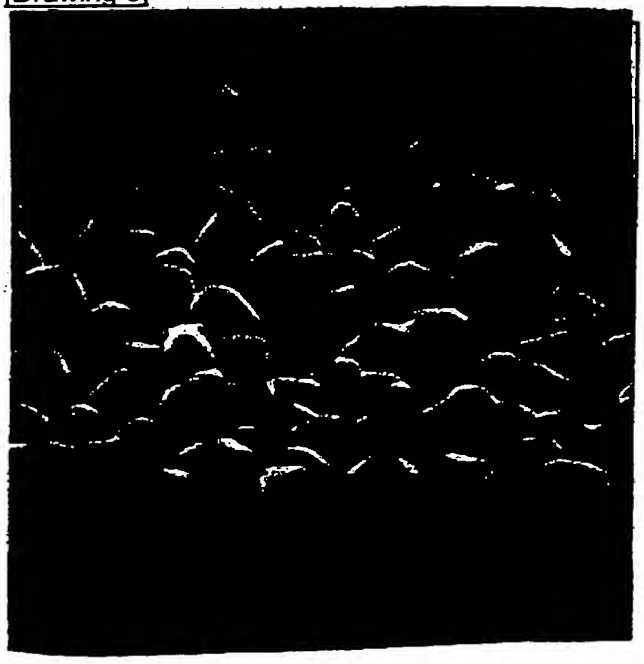
[Drawing 4]



[Drawing 5]

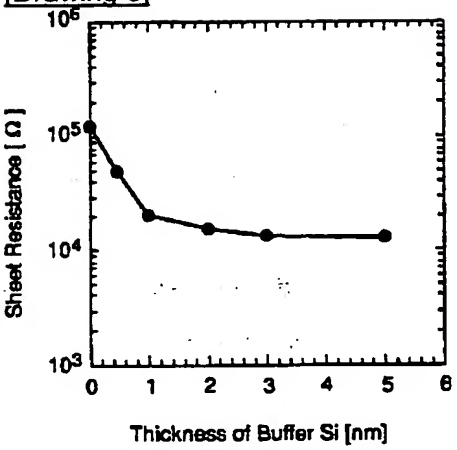


[Drawing 6]



[Drawing 7]

[Drawing 8]



[Translation done.]